TPS6123x 8-A Valley Current Synchronous Boost Converters with Constant Current Output Feature

1 Features

- Up to 97% Efficiency Synchronous Boost
- Up to 3.5-A I_{OUT} for 3.3-V to 5-V Conversion
- 10-A 14-mΩ/14-mΩ Internal Power Switches
- Programmable Constant Output Current
- Output Current Monitor
- 10-µA I_Q under Light Load Condition
- Boost Status Indication
- True disconnection during shutdown
- Fixed 5.1-V Output Voltage (TPS61235P) or Adjustable Output Voltage from 2.9-V to-5.5 V (TPS61236P)
- 1-MHz Switching Frequency
- Softstart, Current Limit, Over Voltage and Over Thermal Protections
- 2.5 mm x 2.5 mm VQFN Package

2 Applications

- Power Banks, Battery Backup Units
- USB Charging Port
- USB Type-C
- Battery Powered USB Hub
- Tablet PCs
- Battery Powered Products

3 Description

The TPS6123x is a high current, high efficiency synchronous boost converter with constant output current feature for single cell Li-Ion and Li-polymer battery powered products, in a wide range of power bank, tablet, and other portable devices. The IC integrates 14-mΩ/14-mΩ power switches and is capable of delivering up to a 3.5-A output current for 3.3-V to 5-V conversion with up to 97% high efficiency. The device supports a programmable constant output current to control power delivery, so to save power path components and lower total system thermal dissipation effectively.

The device only consumes a 10-µA quiescent current under a light load condition, and can report load status to the system, which make it very suitable for Always-On applications. With the TPS6123x, a simple and flexible system design can be achieved, eliminating external power path components, saving PCB space, and reducing BOM cost.

In shutdown, the output is completely disconnected from the input, and current consumption is reduced to less than 1 µA. Other features like soft start control, reverse current blocking, over voltage protection, and thermal shutdown protection are built-in for system safety.

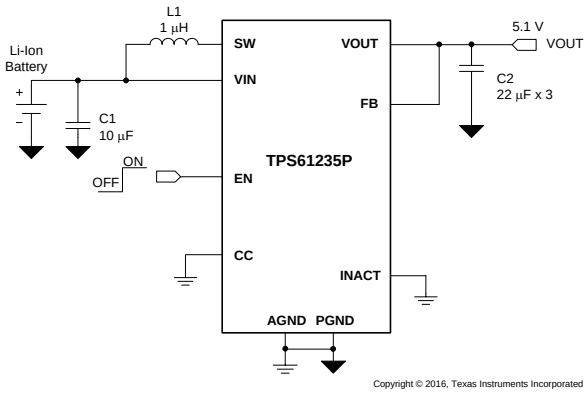
The devices are available in a 2.5-mm x 2.5-mm VQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61235P	VQFN (9)	2.50 mm x 2.50 mm
TPS61236P	VQFN (9)	2.50 mm x 2.50 mm

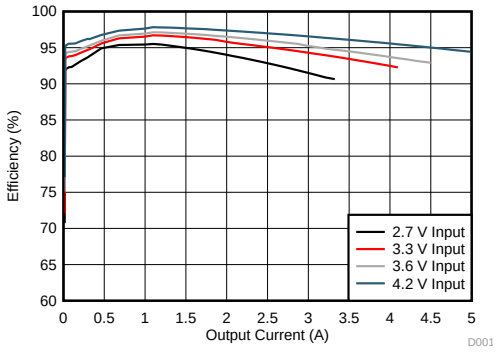
(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS61235P Typical Application



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Typical Application Efficiency (TPS61235P)



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Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Typical Characteristics ... 7
8 Detailed Description ... 9
8.1 Overview ... 9
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 10
8.4 Device Functional Modes ... 15
9 Applications and Implementation ... 16
9.1 Application Information ... 16
9.2 Typical Applications ... 16
10 Power Supply Recommendations ... 26
11 Layout ... 27
11.1 Layout Guidelines ... 27
11.2 Layout Example ... 27
11.3 Thermal Considerations ... 28
12 Device and Documentation Support ... 29
12.1 Device Support ... 29
12.2 Documentation Support ... 29
12.3 Related Links ... 29
12.4 Community Resources ... 29
12.5 Trademarks ... 29
12.6 Electrostatic Discharge Caution ... 29
12.7 Glossary ... 29
13 Mechanical, Packaging, and Orderable Information ... 30

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (Septimber 2015) to Revision A	Page
• Changed part numbers to TPS61235P and TPS61236P for Pb-free nomenclature	1

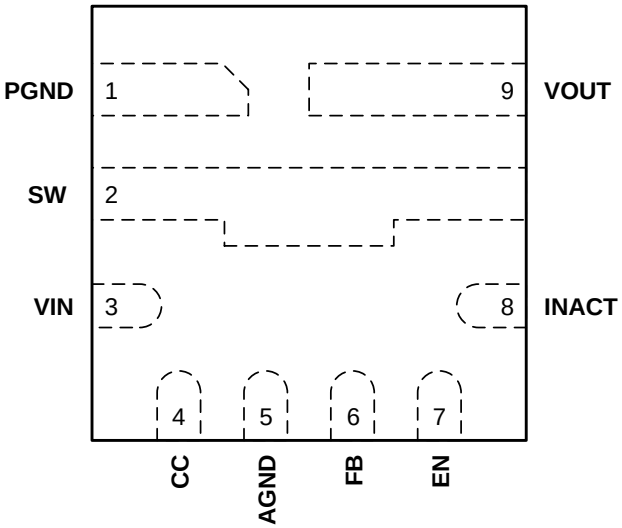
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5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE
TPS61235P	5.1 V
TPS61236P	Adjustable

6 Pin Configuration and Functions

RWL Package
9-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PGND	1	PWR	Power ground.
SW	2	PWR	The switch pin of the boost converter. It is connected to the drain of the internal Power MOSFETs.
VIN	3	I	IC power supply input.
CC	4	I	Constant output current programming pin. Connect a resistor to this pin to program the constant output current. A capacitor should be connected in parallel to stabilize the control loop. Connect this pin to the AGND pin to disable the constant output current function.
AGND	5	I/O	Analog ground.
FB	6	I	Voltage feedback pin of adjustable version (TPS61236P). Must be connected to VOUT pin on fixed output voltage version (TPS61235).
EN	7	I	Enable logic input. Logic high enables the device. Logic low disables the device and puts it in shutdown mode. This pin must be terminated and cannot be left floating. An external pull down resistor connected to this pin is recommended.
INACT	8	O	Load status indication. Open drain output. Can be left float or connected to AGND pin if not used.
VOUT	9	PWR	Boost converter output.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, VOUT, CC, INACT, FB	–0.3	6	V
	SW	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}(1)	Supply voltage at VIN pin	2.3		V_{OUT} – 0.6	V
V_{OUT}	Target output voltage (TPS61235P)		5.1		V
	Target output voltage (TPS61236P)	2.9		5.5	V
L	Effective inductance	0.7	1	1.3	µH
C_I	Effective input capacitance(2)	4.7	10		µF
C_O	Effective output capacitance(2)	20			µF
C_{RCC}	Capacitor parallel with the RCC resistor connected at CC pin	1	10		nF
R_{INACT}	INACT pin pull up resistance		1		MΩ
R_{EN}	EN pin pull down resistance		1		MΩ
T_J	Operating junction temperature	–40		125	°C

(1) The maximum input voltage should be 0.6-V lower than the output voltage in Constant Voltage operation for the TPS6123x to function correctly.
(2) Effective capacitance value. Ceramic capacitor's derating effect under bias should be considered when selecting capacitors.

7.4 Thermal Information

THERMAL METRIC(1)		TPS61235P TPS61236P RWL (VQFN) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	24.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_J = –40°C to 125°C and V_{IN} = 3.6 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage		2.3		V_{OUT} – 0.6	V
V_{UVLO}	Input under voltage lockout	V_{IN} rising		2.2	2.3	V
		Hysteresis		125		mV
I_Q	Quiescent current into VIN	IC enabled, No Load, No switching, V_{OUT} = 5.1 V		5	11	µA
	Quiescent current into VOUT			5	30	µA
I_{SD}	Shutdown current into VIN	IC disabled, T_J = –40°C to 85°C		0.01	3	µA
OUTPUT						
V_{OUT}	Output voltage range	TPS61236P	2.9		5.5	V
	Output voltage	PWM mode, TPS61235P	5.0	5.1	5.2	V
		PFM mode, TPS61235		5.2		V
V_{FB}	Feedback voltage	PWM mode, TPS61236P	1.219	1.244	1.269	V
		PFM mode, TPS61236P		1.256		V
V_{OVP}	Output over voltage protection threshold		5.60	5.80	5.93	V
I_{LKG_FB}	Leakage current into FB pin	TPS61235P, V_{FB} = 5.1 V			4000	nA
		TPS61236P, V_{FB} = 1.244 V			120	nA
I_{LKG_SW}	Leakage current into SW pin	IC disabled, T_J = –40°C to 85°C, V_{SW} = 5.1 V		0.05	2	µA
I_{LKG_VOUT}	Leakage current into VOUT pin	IC disabled, T_J = –40°C to 85°C, V_{OUT} = 5.1 V		0.05	2	µA
	Line regulation	I_{OUT} = 2A, V_{IN} = 2.7 V to 4.5 V, V_{OUT} = 5.1 V		0.06		%/V
	Load regulation	I_{OUT} = 0.5 A to 3 A, V_{IN} = 3.6 V, V_{OUT} = 5.1 V		0.06		%/A
POWER STAGE						
$R_{DS(on)}$	High side MOSFET on resistance	V_{OUT} = 5.1 V		14	30	mΩ
	Low side MOSFET on resistance	V_{OUT} = 5.1 V		14	30	mΩ
f_{sw}	Switching frequency	V_{OUT} = 5.1 V, PWM mode	750	1000	1250	kHz
	Constant output current limit accuracy	R_{CC} = 124 kΩ, T_J = 25°C	–15		15	%
		R_{CC} = 61.9 kΩ, T_J = 25°C	–10		10	%
		R_{CC} = 61.9 kΩ, T_J = –20°C to 125°C	–15		15	%
I_{LIM}	Switch valley current limit	T_J = –20°C to 100°C	6.5	8	9.5	A
I_{LIM_pre}	Precharge mode current limit	V_{OUT} = 0 V, T_J = 0°C to 125°C	0.05	0.25	0.8	A
		V_{OUT} = 2 V		1.3		A
		V_{OUT} = 3 V		1.7		A
I_{INACT_th}	Inactive threshold	V_{OUT} = 5.1 V		50		mA
t_{INACT_delay}	Deglitch delay	V_{OUT} = 5.1 V		15		ms
T_{SD}	Thermal shutdown threshold	T_J rising		140		°C
		Hysteresis		15		°C

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Electrical Characteristics (continued)

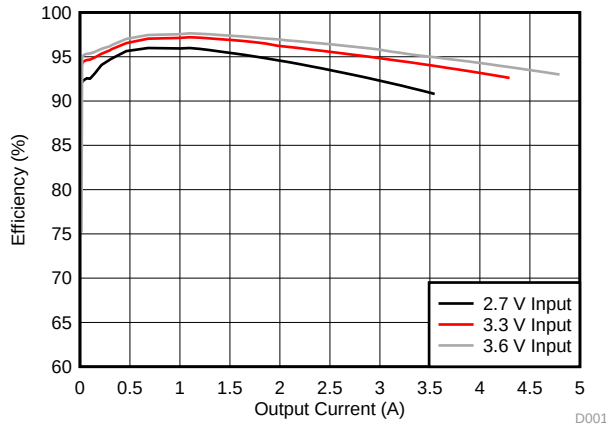
T_J = –40°C to 125°C and V_{IN} = 3.6 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INTERFACE						
V_{EN_H}	EN Logic high input voltage		1.0			V
V_{EN_L}	EN Logic low input voltage				0.4	V
I_{LKG_EN}	EN pin input leakage current	EN pin connected to GND or VIN		0.01	0.3	µA
V_{INACT}	INACT pin output low level voltage	I_{SINK_INACT} = 80 µA			0.4	V

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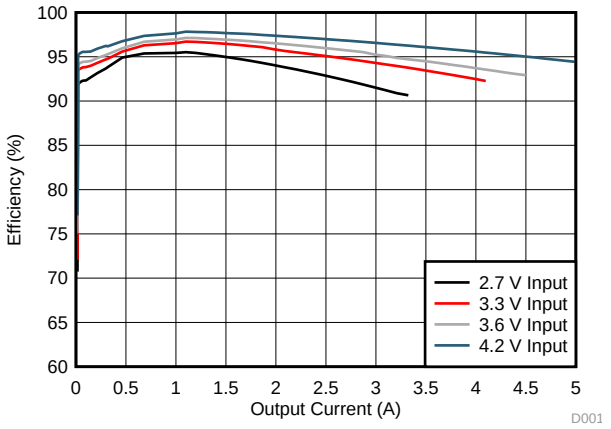
7.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = –40°C to 125 °C, unless otherwise noted.



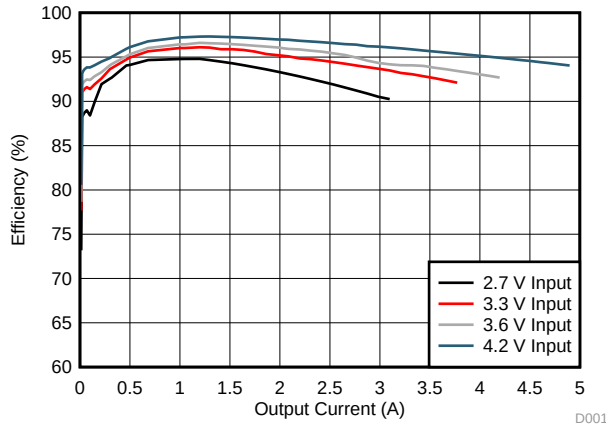
V_{OUT} = 4.5 V (TPS61236P), CC pin connected to GND

Figure 1. Efficiency vs Output Current with Different Inputs



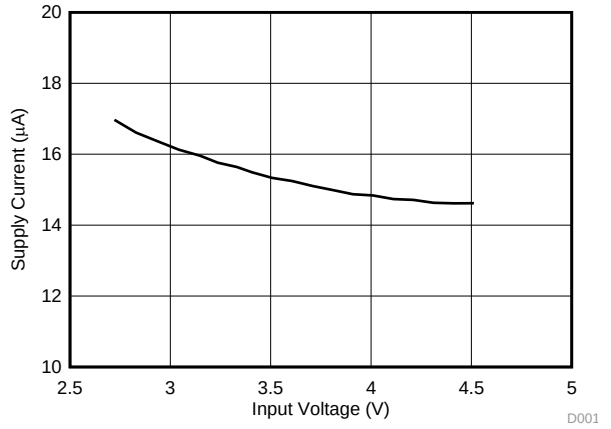
V_{OUT} = 5.1 V (TPS61235P), CC pin connected to GND

Figure 2. Efficiency vs Output Current with Different Inputs



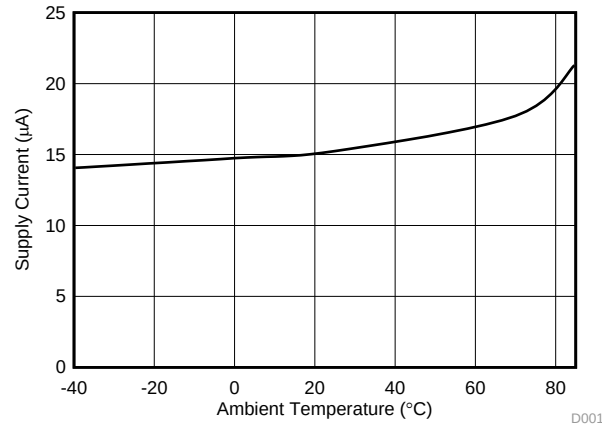
V_{OUT} = 5.5 V (TPS61236P), CC pin connected to GND

Figure 3. Efficiency vs Output Current with Different Inputs



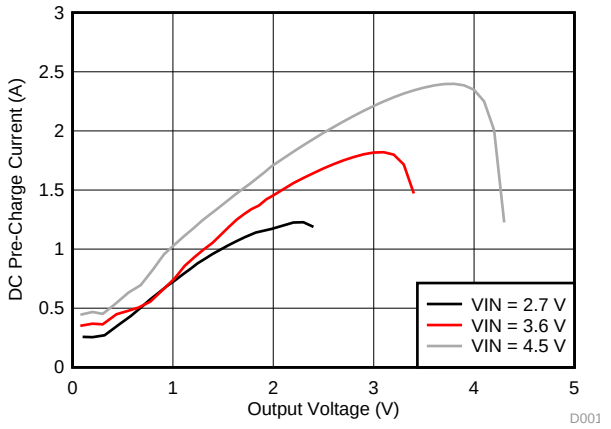
V_{OUT} = 5.1 V (TPS61235P), No Load, T_A = 25°C

Figure 4. No Load Supply Current vs Input Voltage



V_{OUT} = 5.1 V (TPS61235P), V_{IN} = 3.6 V, No Load

Figure 5. No Load Supply Current vs Ambient Temperature

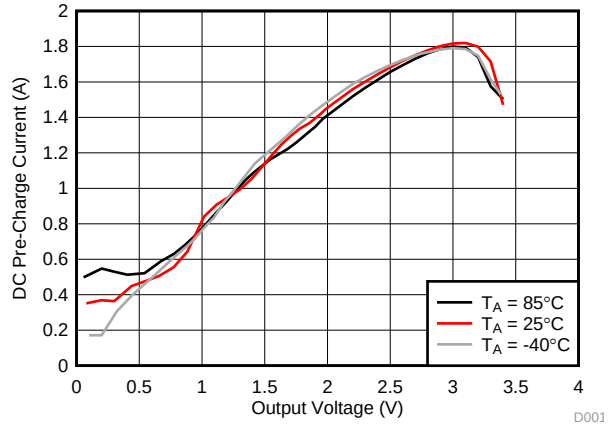


T_A = 25°C

Figure 6. DC Pre-Charge Current vs Output Voltage

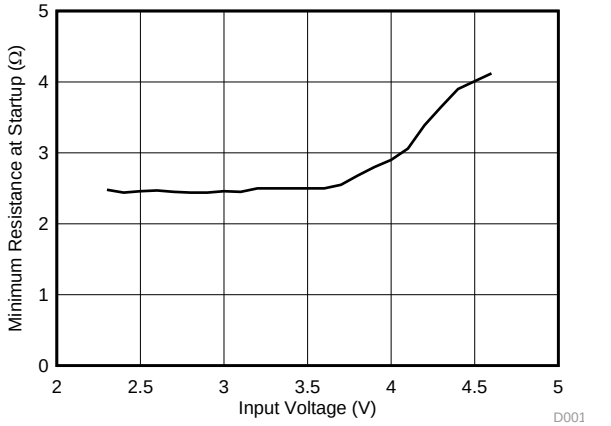
Typical Characteristics (continued)

V_{IN} = 3.6 V, V_{OUT} = 5.0 V, T_J = –40°C to 125 °C, unless otherwise noted.



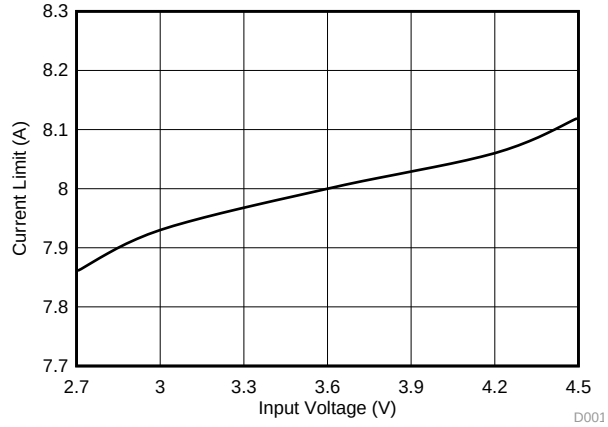
3.6-V Input

Figure 7. DC Pre-Charge Current vs Output Voltage



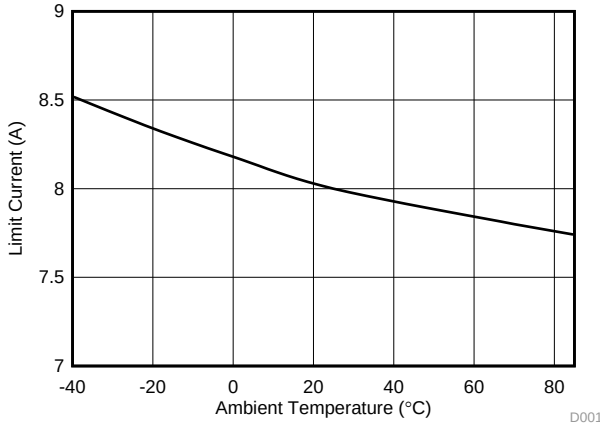
V_{OUT} = 5.1 V (TPS61235P), CC pin connected to GND, T_A = 25°C

Figure 8. Minimum Load Resistance at Startup



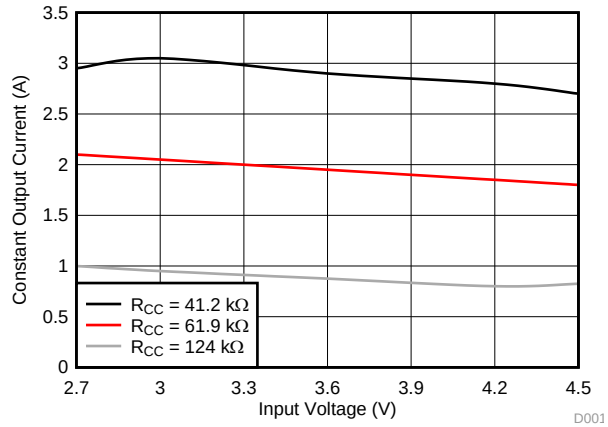
T_A = 25°C

Figure 9. Current Limit vs Input Voltage



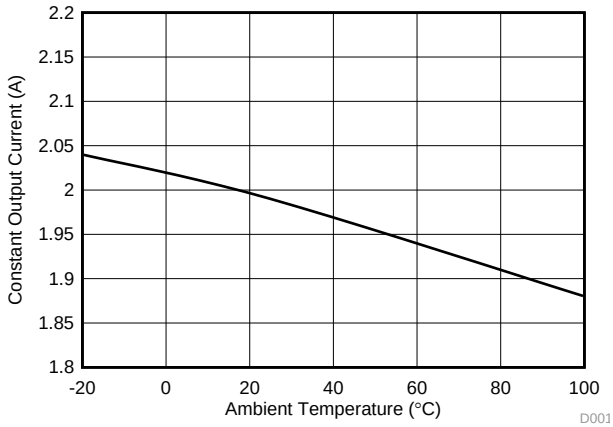
V_{IN} = 3.6 V

Figure 10. Current Limit vs Ambient Temperature



V_{OUT} = 5.1 V (TPS61235P), T_A = 25°C

Figure 11. Constant Output Current vs Input Voltage



V_{OUT} = 5.1 V (TPS61235P), R_{CC} = 61.9 kΩ (CC current set to 2 A)

Figure 12. Constant Output Current vs Ambient Temperature

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8 Detailed Description

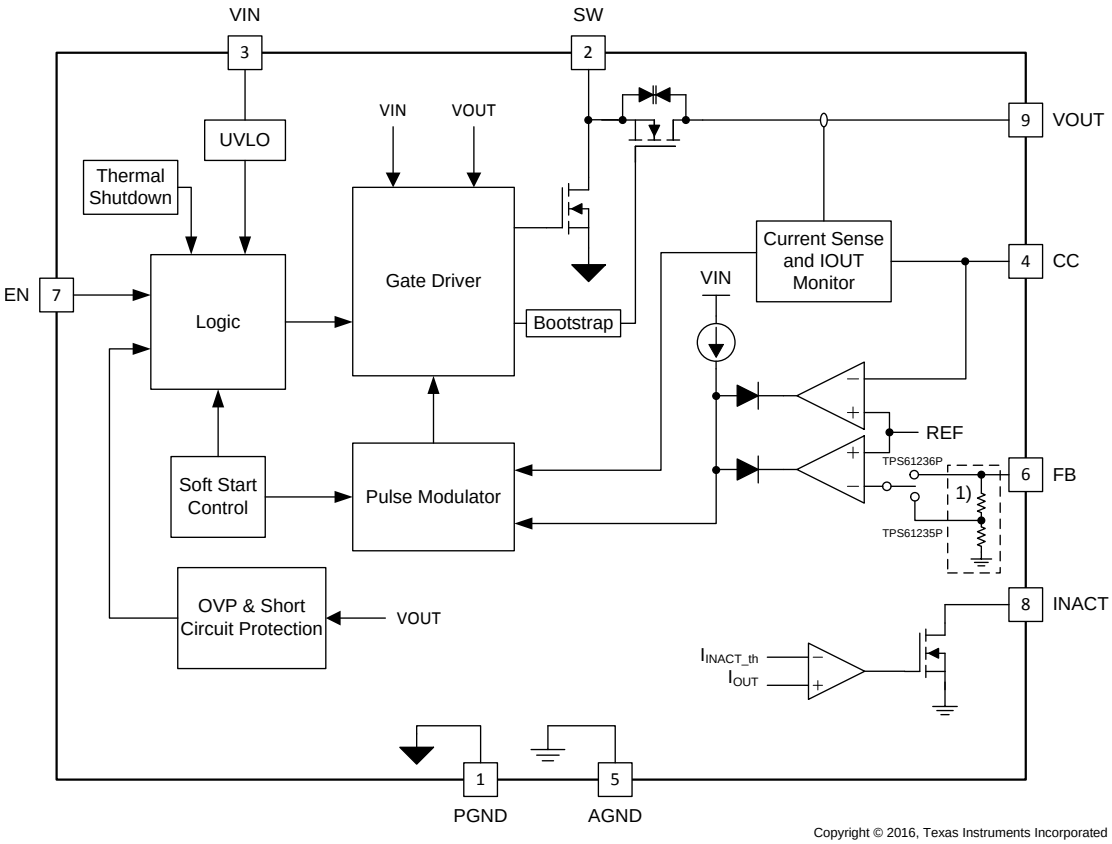
8.1 Overview

The TPS6123x is a high current, high efficiency synchronous boost converter with constant current output feature. It is optimized for single cell Li-Ion and Li-polymer battery powered products, in a wide range of power bank, tablet, and other portable devices. The converter integrates 14-mΩ /14-mΩ power switches and is capable of delivering more than 3.5-A output current for 3.3-V to 5-V conversion. The low $R_{ds(on)}$ of the internal power switches enables up to 97% power conversion efficiency.

The TPS6123x has two regulation loops, one is the output voltage regulation loop as the normal boost converters have, and the other is the output current regulation loop. An external resistor can be used to program the maximum output current, and once the output current reaches the programmed value, the current loop kicks in to regulate the output current. The TPS6123x can also indicate the load status. These features can simplify system design, eliminate external power path components like a load switch, and achieve much lower system thermal dissipation and improve the total power conversion effectively.

The TPS6123x also consumes only 10-µA quiescent current under a light load condition. This low quiescent current together with the load status indication function makes the device very suitable for Always-On applications. For example, for a power bank application, the TPS6123x can remain always on and report load status to the system controller.

8.2 Functional Block Diagram



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(1) Internal FB resistor divider is implemented in TPS61235P only.

8.3 Feature Description

8.3.1 Boost Controller Operation

The TPS6123x synchronous boost converter typically operates at a quasi-constant 1-MHz frequency Pulse Width Modulation (PWM) at moderate to heavy load, which allows the use of small inductors and capacitors to achieve a small solution size. At light load, it operates in power-save mode with Pulse Frequency Modulation (PFM) for improved efficiency.

During PWM operation, the converter uses a quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation. Based on the V_{IN} /V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side NMOS switch is turned on and the inductor current ramps up to a peak current that is determined by the on-time and the inductance. Once the on-time has expired, the low-side switch is turned off and the rectifying NMOS switch is turned on. The inductor current decays until reaching the valley current threshold which is determined by internal control loops. Once this occurs, the on-time is set again to turn the low-side switch back on and the cycle is repeated. Internal loop compensation is implemented to simplify the design process while minimizing the number of external components. A bootstrap circuit is built in to drive the rectifying NMOS switch. Figure 13 illustrates the PWM mode operation.

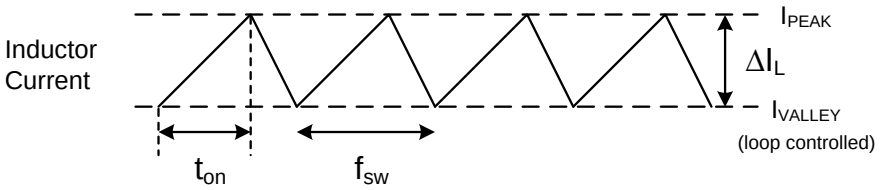


Figure 13. PWM Mode Operation Illustration

Under a light load condition, the converter works in Pulse Frequency Modulation (PFM) mode. In this mode, the boost converter switches and ramps up the output voltage until V_{OUT} reaches the PFM threshold. Then it stops switching and consumes less quiescent current. It resumes switching when the output voltage drops below the threshold. The converter exits PFM mode when the output current can no longer be supported in this mode. Refer to Figure 14 for PFM mode operation details.

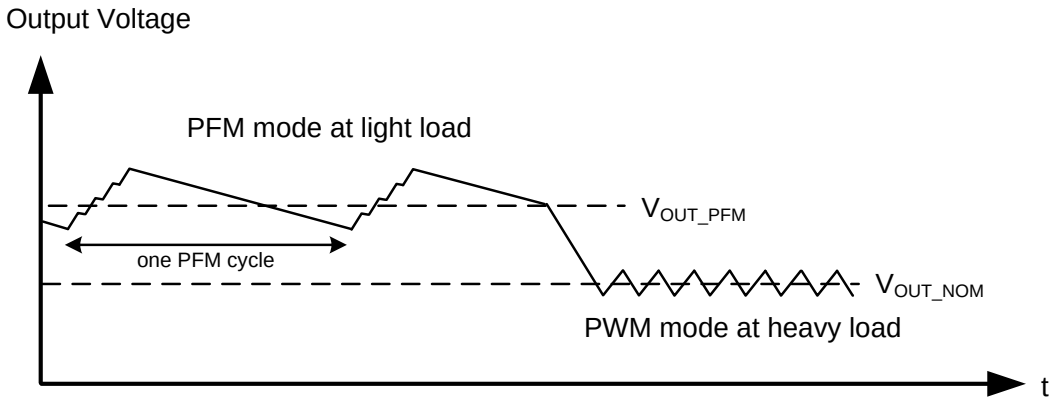


Figure 14. PFM Mode Operation Illustration

8.3.2 Soft Start

The TPS6123x integrates an internal soft start circuit which controls ramp up of the output voltage and prevents the converter from inrush current during start-up.

When the device is enabled, the rectifying switch is turned on to charge the output capacitor to the input voltage. This is called the pre-charge phase. During the phase, the output current is limited to the pre-charge current limit I_{LIM_pre}, which is proportional to the output voltage. The pre-charge current increases when the output voltage gets higher.

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Feature Description (continued)

Once the output capacitor is charged close to the input voltage, the converter starts switching. This is called the start-up switching phase. During the phase, the converter steps up the voltage to its nominal output voltage by following an internal ramp up reference voltage, which ramps up in around 3 ms (typ.) to its final value. The current limit function is activated in this phase.

Because of the current limitation during the pre-charge phase, the TPS6123x may not be able to start up under a heavy load condition. It is recommended to apply no load or a light load during the startup process, and apply the full load only after the TPS6123x starts up successfully. Refer to Figure 8 for the recommended minimum load resistance.

8.3.3 Enable and Disable

An external logic signal at the EN pin can enable and disable the device.

The TPS6123x device starts operation when EN is set high and starts up with the soft-start process. For proper operation, the EN pin must be terminated and must not be left floating. Pulling EN low forces the device into shutdown, with a shutdown current of typically 0.01 µA. In shutdown mode, a true disconnection between input and output is implemented. It can prevent current from input to output, or reverse current from output to input.

8.3.4 Constant Output Voltage and Constant Output Current Operations

Normally a boost converter only regulates its output voltage, but for the TPS6123x, it is different. There are two regulation loops for the device. One loop regulates the output voltage, and it is called CV (Constant Voltage) operation; the other regulates the output current, and it is called CC (Constant Current) operation.

8.3.4.1 Constant Voltage Operation

Before the output current reaches the constant current value programmed by an external resistor at the CC pin, the voltage regulation loop dominates. The output voltage is monitored via external or internal feedback network resistors at the FB pin. An error amplifier compares the feedback voltage to an internal reference voltage V_{REF} and adjusts the inductor current valley accordingly. In this way, the TPS6123x operates as a normal boost converter to regulate the output voltage.

During CV operation, the maximum V_{IN} should be 0.6-V below V_{OUT} to keep the output voltage well regulated. The TPS6123x may enter into pass-through operation prematurely when V_{IN} is close to but still below V_{OUT}, and exists when V_{IN} is below the threshold with a hysteresis. When in pass-through operation, the boost converter stops switching and keeps the rectifying switch on, so the input voltage can pass through the external inductor and internal rectifying switch to the output. The output current capability becomes lower and is limited by the pre-charge current limit I_{LIM_pre} of the rectifying switch. More than 0.4-V under-voltage of V_{OUT} may occur due to the premature pass-through operation and the hysteresis of existing. If the under-voltage is not acceptable, the maximum V_{IN} should be limited to 0.6-V below V_{OUT} , which gives enough margin to avoid the pass-through operation.

8.3.4.2 Output Current Monitor

During the CV operation, the output current can be monitored at the CC pin. In the TPS6123x, the inductor current is sensed through the rectifying switch during the off-time of each switching cycle. The device then builds a current signal which is 1/K times the sensed current and feeds it to the CC pin during off-time. As a result, the CC pin voltage, V_{CC}, is proportional to the average output current as Equation 1 shows.

$$V_{CC} = \frac{I_{OUT}}{K} \cdot R_{CC} \quad (1)$$

Where:

V_{CC} is the voltage at the CC pin,

I_{OUT} is the output current,

K is the coefficient between the output current and the internal built current signal, K = 100,000,

R_{CC} is the resistor connected at the CC pin.

A capacitor must be connected in parallel with R_{CC} to average the CC pin voltage and also stabilize the control loop. Normally a 10-nF capacitor is recommended. A larger capacitor at the CC pin will smooth the CC voltage better, and also slow down the loop response.

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Feature Description (continued)

The CC pin can be connected to ground to disable the output current monitor function, and it will not affect the CV operation.

8.3.4.3 Constant Current Operation

As Equation 1 shows, the CC pin voltage is proportional to the output current. The TPS6123x monitors the CC pin voltage and compares it to an internal reference voltage V_{REF}, which is 1.244 V typically. When V_{CC} exceeds V_{REF}, the CC regulation loop kicks in and pulls the inductor current valley to a lower value so to keep the CC pin voltage at V_{REF}. Equally, the output current is regulated at the set value as Equation 2.

$$I_{OUT_CC} = \frac{V_{REF}}{R_{CC}} \cdot K \quad (2)$$

Where:

I_{OUT_CC} is the set constant output current,
V_{REF} is the internal reference voltage, 1.244 V typically,
R_{CC} is the resistor connected at the CC pin,
K is the coefficient between the output current and the internal built current signal, K = 100,000.

If the load current is higher than the CC setting, the output voltage drops. A balance can be achieved if the load decreases and matches the CC current before V_{OUT} is pulled below input voltage. In the balance status, the TPS6123x can keep CC operation, output the constant current, and maintain the output voltage at the balanced level. If the output voltage is pulled below the input voltage by a strong load before the balance is achieved, the device exits CC operation and enters into start-up process, where the output current is limited by I_{LIM_pre} instead of the CC value. If the load is still higher than I_{LIM_pre}, the device will be stuck in the pre-charge phase; otherwise, the device can complete the pre-charge phase, but its output voltage will be pulled down again in the switching phase due to the limited output current, so an oscillation may happen.

In order to avoid the potential oscillation, the CC operation is only recommended for pure resistive loads or load devices with dynamic power management function. For a resistive load, its resistance should be higher than V_{IN} / I_{OUT_CC}; for a load device with dynamic power management function, which can regulate its input voltage to a set value, a higher set voltage than V_{IN} of the TPS6123x is suggested. By doing this, a balance can be achieved before the output voltage is pulled below the input voltage, so to avoid the TPS6123x entering into the startup process.

For effective CC operation, a capacitor must be connected in parallel with R_{CC} at CC pin, and the CC value should be set lower than the maximum output capability of the converter; otherwise, the TPS6123x will trigger the over current protection first and fail to regulate the output current. Refer to the *Over Current Protection* section for details.

The CC operation can be disabled by shorting the CC pin to ground. By doing so, the CC loop is disabled, so the TPS6123x works as a normal boost converter to regulate the output voltage, and its maximum output current capability is decided by the internal current limit.

8.3.5 Over Current Protection

To protect the device from over load condition, an internal cycle-by-cycle current limit is implemented. Once the inductor valley current reaches the internal current limit, the protection is triggered and it clamps the valley current at the limit I_{LIM} until next cycle comes.

Figure 15 illustrates the valley current limit scheme. The average of the rectifier ripple current equals the output current, $I_{OUT(DC)}$. When the load current increases, the loop increases the valley current accordingly. If the valley current is increased above I_{LIM}, the off-time will be extended until the valley drops to I_{LIM}. Then the next cycle begins.

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Feature Description (continued)

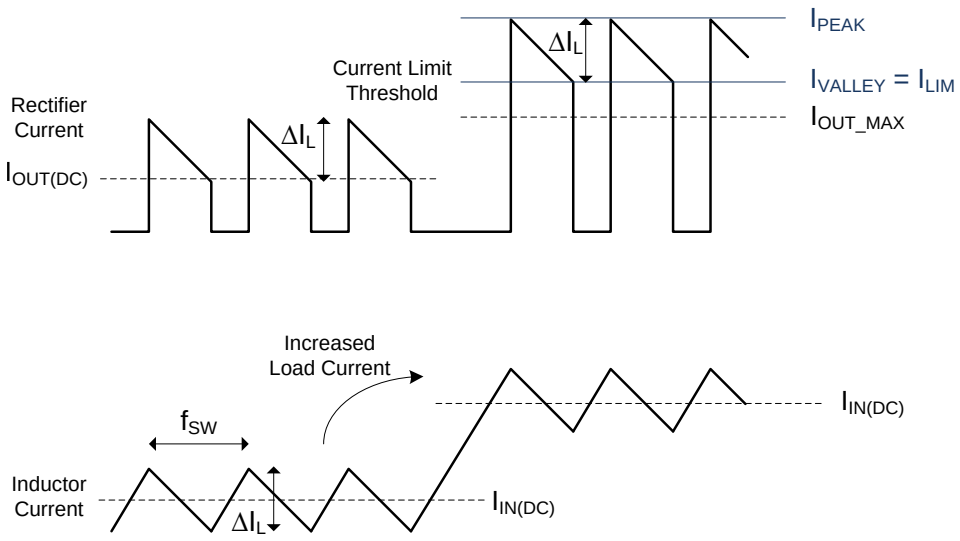


Figure 15. Current Limit Operation

The maximum output current, I_{OUT_MAX}, before the device enters into over current protection is decided by its operation condition and the switch current limit threshold. It can be calculated by using the following equations.

$$I_{OUT_MAX} = (1-D)\cdot\left(I_{LIM} + \frac{\Delta I_L}{2}\right) \quad (3)$$

$$\Delta I_L = \frac{V_{IN}\cdot D}{L\cdot f_{sw}} \quad (4)$$

$$D = 1 - \frac{V_{IN}\cdot \eta}{V_{OUT}} \quad (5)$$

Where:

D is the duty cycle of the boost converter,
I_{LIM} is the switch valley current limit threshold,
ΔI_L is the inductor current ripple,
L is the inductor value,
f_{SW} is the switching frequency,
η is the conversion efficiency under the operation condition.

To estimate the maximum output current capability in the worst case, the minimum input voltage value, highest f_{SW} value, and minimum I_{LIM} value should be used for the calculation. And η should be the efficiency under this minimum V_{IN} operation condition.

When the current limit is reached, the output voltage decreases during further load increases. If the output voltage drops below the input voltage, the device enters into the start-up process.

8.3.6 Load Status Indication

The TPS6123x can indicate load status by the INACT pin. The INACT pin is an open drain output and should be connected to a pull-up resistor. The INACT pin outputs high impedance when the boost converter works under inactive status (no load or light load status), and it outputs low logic when the boost converter works under active status (moderate load or heavy load status).

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Feature Description (continued)

Load status is defined by operation mode and output current. When the converter works in PFM mode with I_{OUT} lower than the threshold I_{INACT_th} for 16 PFM cycles, the boost enters inactive status. One PFM cycle is defined from the time the boost starts switching to ramp up the output voltage to the time it resumes switching after the output voltage drops below the PFM threshold, as shown in Figure 14. Once the output current is detected higher than I_{INACT_th} or the converter exits PFM mode, the boost enters active status. There is 10-ms typical deglitch time when the INACT pin changes its output.

This indication function can report load status to a system controller, like an MCU. For example, it can be used to realize the load insert detection in a power bank application, where the TPS6123x can be kept always on while consuming only 10-µA quiescent current. When a load is applied, the TPS6123x detects the load and pulls the INACT pin low to wake up the MCU. It eliminates the need for external load detection circuitry and simplifies the system design.

8.3.7 Under voltage Lockout

Under voltage lockout prevents operation of the device at input voltages below typical 2.1-V. When the input voltage is below the under voltage threshold, the device is shut down and the internal switch FETs are turned off. If the input voltage rises by under voltage lockout hysteresis, the IC restarts.

8.3.8 Over Voltage Protection and Reverse Current Block

When the device detects the output voltage above the threshold V_{OVP}, the over voltage protection will be triggered. The device stops switching and turn off the low side switch and rectifying switch. The voltage at output is blocked to input, and there is no reverse current. When the output voltage falls below the OVP threshold, the device resumes normal operation.

8.3.9 Short Circuit Protection

If the output voltage is detected lower than the input voltage during operation, the TPS6123x will enter into the pre-charge phase of the startup process. The output current is limited to I_{LIM_pre} by the rectifying switch, which is 0.25-A typical when V_{OUT} is short to ground. When the short circuit event is removed, the TPS6123x will start up automatically.

Short circuit protection is only valid when the input voltage is below 4.5 V. If the input voltage is higher than 4.5 V, a long term short to ground event may damage the device.

8.3.10 Thermal Shutdown

The TPS6123x has a built-in temperature sensor which monitors the internal junction temperature, T_J. If the junction temperature exceeds the threshold (140°C typical), the device goes into thermal shutdown, and the high-side and low-side MOSFETs are turned off. When the junction temperature falls below the thermal shutdown minus its hysteresis (15°C typical), the device resumes operation.

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8.4 Device Functional Modes

8.4.1 PWM Mode

The TPS6123x boost converter operates at a quasi-constant 1-MHz frequency PWM mode at moderate to heavy load currents. Refer to the *Boost Controller Operation* section for details.

8.4.2 PFM Mode

The TPS6123x works in PFM mode under light load conditions to improve light load efficiency. Refer to the *Boost Controller Operation* section for details.

8.4.3 CV Mode and CC Mode

A resistor at the CC pin can program the maximum output current of the TPS6123x. Before the output current reaches the programmed value, the TPS6123x works in CV (Constant Voltage) mode as a normal boost converter. When the output current reaches the programmed value, the TPS6123x works in CC (Constant Current) mode. Refer to the *Constant Output Voltage and Constant Output Current Operations* section for details.

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6123x family is designed to operate from an input voltage supply range from 2.3-V to (V_{OUT} – 0.6)-V, and the maximum output voltage can be up to 5.5-V. The device operates in PWM mode under medium to heavy load conditions and in power save mode under light load condition. In PWM mode, the TPS6123x converter operates with 1-MHz switching frequency which provides a controlled frequency variation over the input voltage range. As load current decreases, the converter enters PFM mode, reducing switching frequency and minimizing IC quiescent current to achieve high efficiency over the entire load current range. The TPS6123x also supports a constant current output feature to limit the maximum output current at a programmed value.

9.2 Typical Applications

9.2.1 TPS61236P 3-V to 4.35-V Input, 5-V Output Voltage, 3-A Maximum Output Current

This example illustrates how to use the TPS61236P to generate a 5-V output voltage from a Li-ion battery input and how to use the CC function to limit maximum output current to 3-A for the entire input voltage range.

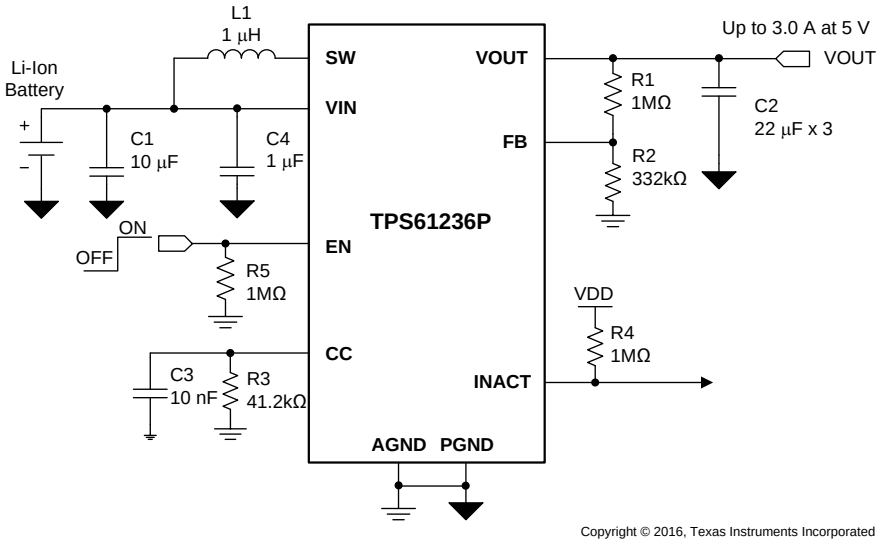


Figure 16. TPS61236P 5-V Output with 3-A Constant Output Current

9.2.1.1 Design Requirements

The design parameters for the TPS61236P 5-V 3-A constant output current design are listed in Table 1.

Table 1. TPS61236P 5-V 3-A Constant Output Current Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	3 V to 4.35 V
Output voltage	5 V
Output current limit	3 A
Operating frequency	1 MHz

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9.2.1.2 Detailed Design Procedure

The following sections describe the selection process of the external components. The following table summaries the final component selections.

Table 2. List of Components for TPS61236P 5-V Output with 3-A Constant Output Current Application

REFERENCE	DESCRIPTION	MANUFACTURER(1)
L1	1.0 µH, Power Inductor, XAL7030	Coilcraft
C1	10 µF 6.3 V, 0603, X5R ceramic, GRM188R60J106ME84	Murata
C2	3 × 22 µF 10 V, 0805, X5R ceramic, GRM21BR61A226ME44	Murata
C3	10 nF, 50 V, 0603, X5R ceramic, GRM188R61H103KA01D	Murata
C4	1 µF, 6.3 V, 0402, X5R ceramic, GRM152R60J105ME15	Murata
R1	1 MΩ, Resistor, Chip, 1/10W, 1%	Rohm
R2	332 kΩ, Resistor, Chip, 1/10W, 0.5%	Rohm
R3	41.2 kΩ, Resistor, Chip, 1/10W, 0.5%	Rohm
R4	1 MΩ, Resistor, Chip, 1/10W, 1%	Rohm
R5	1 MΩ, Resistor, Chip, 1/10W, 1%	Rohm

(1) See Third-party Products Disclaimer

9.2.1.2.1 Programming the Output Voltage

The TPS61236P's output voltage needs to be programmed via an external voltage divider at the FB pin, as shown in Figure 16.

By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{FB}. The following equation can be used to calculate R1 and R2.

$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) = 1.244V \times (1 + \frac{R1}{R2}) \quad (6)$$

For the best accuracy, the current following through R2 should be 100 times larger than FB pin leakage current. Changing R2 towards a lower value increases the robustness against noise injection. Changing R2 towards higher values reduces the FB divider current for achieving the highest efficiency at low load currents.

For the fixed output voltage version, TPS61235P, the FB pin must be tied to the output directly.

In this example, 1-MΩ and 332-kΩ resistors are selected for R1 and R2. High accuracy like 0.5% resistors are recommended for better output voltage accuracy.

9.2.1.2.2 Program the Constant Output Current

The TPS6123x's constant output current can be programmed via an external resistor R_{CC} at the CC pin.

Because the TPS6123x has an internal current limit function to protect the IC from over load situations, a user should make sure the constant output current is set within the device's maximum load capability. If the constant current is set too high, the output current will be limited by internal protection circuitry and cannot reach the set value.

The maximum output capability is determined by the input to output voltage ratio and the internal current limit I_{LIM}. Refer to Equation 3, Equation 4, and Equation 5 for the maximum output current calculation. The minimum input voltage, minimum current limit value, and maximum switching frequency value shall be used for the worst case calculation.

In this example, the minimum input voltage is 3-V and output voltage is 5-V. The efficiency η can be estimated as 85% for the worst case condition. By checking the specification table, the minimum I_{LIM} value is 6.5-A, and maximum switching frequency f_{SW} is 1250-kHz, so the calculation result of the maximum output current under the worse case condition is 3.6-A.

After calculation, the 3-A constant current target is within the maximum output current range, so the user can set it. Equation 2 can be used to select R_{CC} (R3 in Figure 16). In this example, the calculation result of R3 is 41.47-kΩ. A 1% accuracy 41.2-kΩ resistor is selected. By using it, the constant output current can be regulated at 3-A typically.

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C3 must be connected in parallel with R3 to average the CC pin voltage and also stabilize the control loop. A larger capacitor can smooth the CC voltage better, and also slow down the loop response. Normally a 10-nF capacitor is recommended.

If the Constant Current function is not needed, the user can simply connect the CC pin to ground to disable it. Under this configuration, the TPS6123x works as a normal boost converter, and its maximum output current is decided by the internal current limit circuitry.

9.2.1.2.3 Inductor and Capacitor Selection

A boost converter requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. Please refer to the following sections to select the inductor and capacitor. Also refer to the *Recommended Operating Conditions* for operation recommendations.

9.2.1.2.3.1 Inductor Selection

Because a 1-µH inductor normally has a higher current rating and smaller form factor than inductors of higher values, the TPS6123x is optimized for 1-µH inductor operation. Inductors of other values may cause control loop instability and so are not recommended.

It is advisable to select an inductor with a saturation current I_{SAT} higher than the possible peak current flowing through the inductor. The inductor's current rating I_{RMS} should be higher than the average input current. The inductor peak current varies as a function of the load, the input and output voltages, and can be estimated by using Equation 7.

$$I_{L_peak} = I_{IN_avg} + \frac{\Delta I_L}{2} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \cdot D}{2 \cdot L \cdot f_{sw}} \quad (7)$$

Where:

D is the duty cycle, and can be calculated by using Equation 5.

When estimating inductor peak current and average input current, the minimum input voltage, maximum output current, and minimum switching frequency in the application should be used for the worst case calculation. In this example, the minimum V_{IN} is 3.0-V, maximum I_{OUT} is 3-A, and minimum f_{sw} is 750-kHz, so the inductor peak current result is 6.9-A, and the average input current is 5.9-A with an 85% efficiency estimation.

Selecting an inductor with insufficient saturation current can lead to excessive peak current in the converter. This could eventually harm the device and reduce reliability. To leave enough margin, it is recommended to choose saturation current 20% to 30% higher than I_{L_PEAK}.

The following inductors are recommended to be used in designs if the current rating allows.

Table 3. List of Inductors

INDUCTANCE [µH]	ISAT [A]	IRMS [A]	DC RESISTANCE [mΩ]	PART NUMBER	MANUFACTURER(1)
1	28	21.8	4.55	XAL7030-102ME	Coilcraft
1	14.1	13	7.1	SPM6530T-1R0M120	TDK
1	19	11	9	FDSD0630-H-1R0M	TOKO
1	11	6	23	SPM5020T-1R0M	TDK

(1) See Third-party Products Disclaimer

9.2.1.2.3.2 Output Capacitor Selection

For the output capacitor, it is recommended to use small X5R or X7R ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic capacitor of 1-µF or 0.1-µF in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC.

The TPS6123x requires at least 20-µF effective capacitance at output for stability consideration. Care must be taken when evaluating a capacitor's derating under bias. The bias can significantly reduce the effective capacitance. Ceramic capacitors can have losses of as much as 50% of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. In this example, three 22-µF capacitors of 10-V rating are used.

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The ESR impact on the output ripple must be considered as well if tantalum or electrolytic capacitors are used. Assuming there is enough capacitance such that the ripple due to the capacitance can be ignored, the ESR needed to limit the V_{Ripple} is:

$$V_{Ripple(ESR)} = I_{L(PEAK)} \times ESR \quad (8)$$

9.2.1.2.3.3 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. The required minimum effective capacitance at input for the TPS6123x is 4.7-µF. Considering the capacitor's derating under bias, a 10-µF input capacitor is recommended, and a 22-µF input capacitor should be sufficient for most applications. There is no limitation to use larger capacitors. It is recommended to put the input capacitor close to the VIN and PGND pins of the IC. If, for any reason, the input capacitor cannot be placed close to the IC, putting a small ceramic capacitor of 1-µF or 0.1-µF close to the IC's VIN pin and ground pin is recommended.

Take care when a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter. A load step at the output may cause ringing at the VIN pin due to the inductance of the long wires. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional bulk capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source to reduce ringing.

9.2.1.2.4 Loop Stability, Feed Forward Capacitor

One approach of stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple, $V_{Ripple(OUT)}$

When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

Load transient response is another approach to check loop stability. During the load transient recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

To improve output voltage undershoot and overshoot performance during heavy load transient such as a 2-A load step transient, a feed forward capacitor C_{ff} in parallel with R1 is recommended, as shown in Figure 17. The feed forward capacitor increases the loop bandwidth by adding a zero, so to achieve smaller output voltage undershoot, as shown in Figure 25. A 10-pF capacitor is suitable for most applications of the TPS6123x. See Application Note SLVA289 for more application notes of feed forward capacitor.

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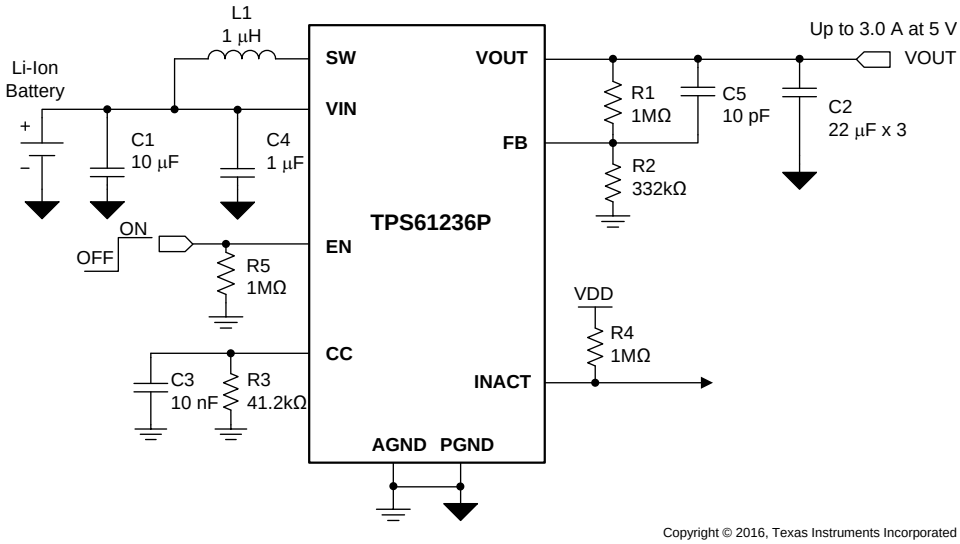


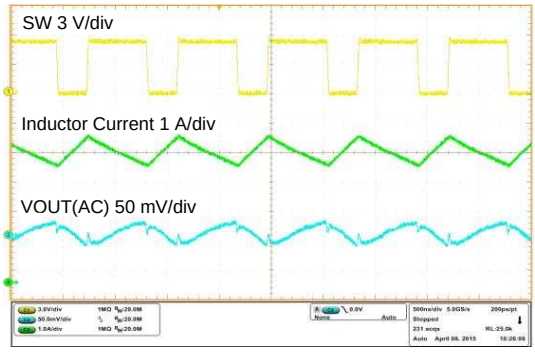
Figure 17. TPS61236P with C_{ff}

9.2.1.2.5 INACT Pin Pull-up Resistor

The INACT pin can be used to report boost converter loading status to the MCU. It is an open drain output and should be connected with a pull up resistor. Normally a 1-MΩ resistor is recommended for the pull up resistor.

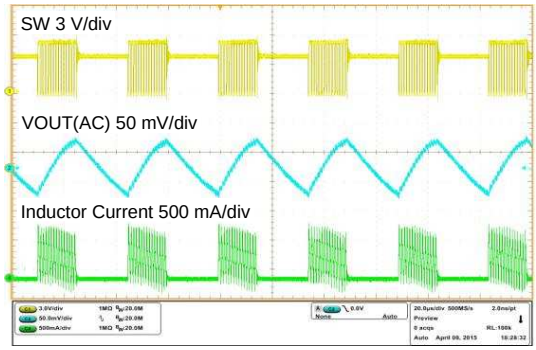
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9.2.1.3 TPS61236P 5-V Output Application Curves



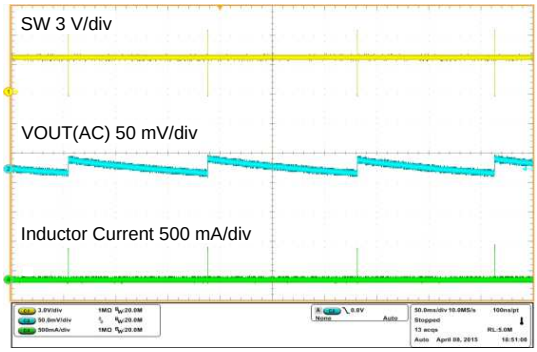
VIN = 3.6 V, VOUT = 5 V, IOUT = 3.1 A

Figure 18. Switching Waveforms in PWM Mode



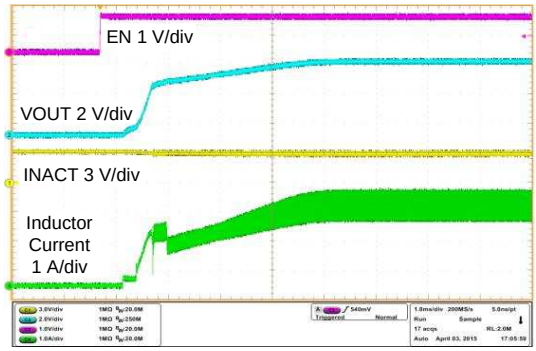
VIN = 3.6 V, VOUT = 5 V, IOUT = 100 mA

Figure 19. Switching Waveforms in PFM Mode



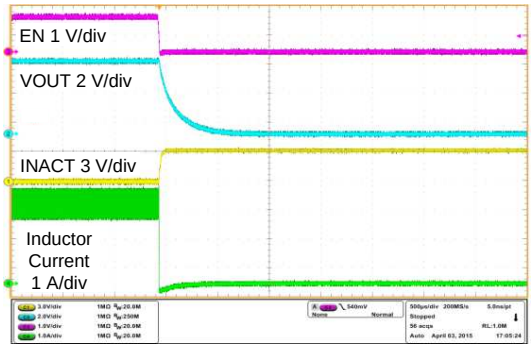
VIN = 3.6 V, VOUT = 5 V, IOUT = 0 mA

Figure 20. Switching Waveforms in PFM Mode



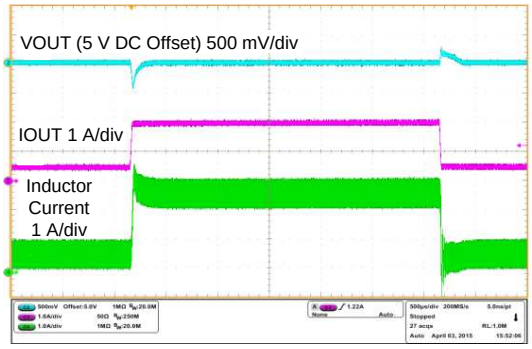
VIN = 3.6 V, VOUT = 5 V, R_L = 2.5 Ω

Figure 21. Startup



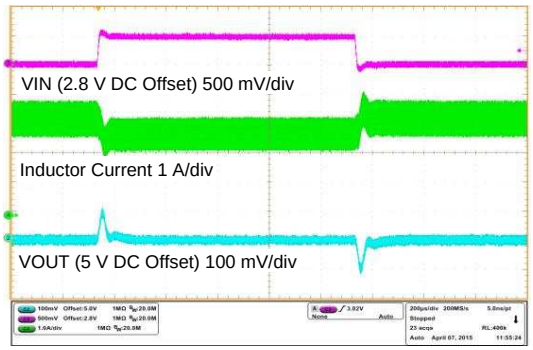
VIN = 3.6 V, VOUT = 5 V, R_L = 2.5 Ω

Figure 22. Shutdown Waveforms



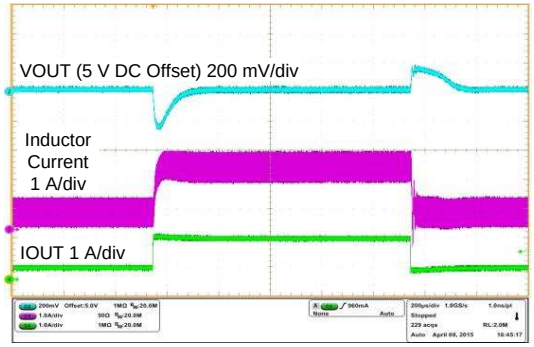
VIN = 3.6 V, VOUT = 5 V, IOUT = 500 mA to 2 A

Figure 23. Load Transient Response



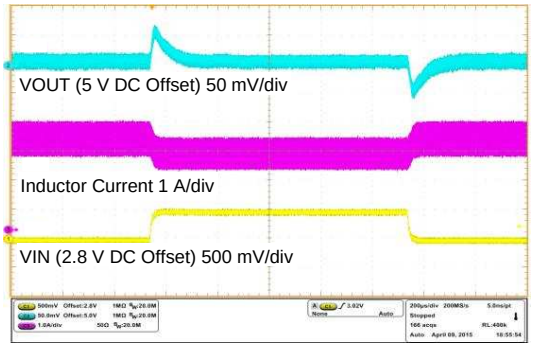
VIN = 2.8 V to 3.3 V, VOUT = 5 V, IOUT = 2 A

Figure 24. Line Transient Response



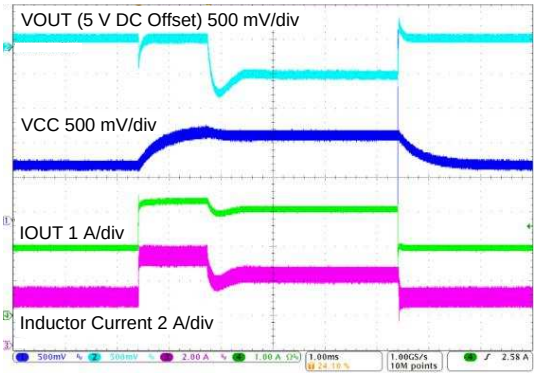
VIN = 3.6 V, VOUT = 5 V, IOUT = 500 mA to 2 A, Cff = 10 pF

Figure 25. Load Transient Response with Cff



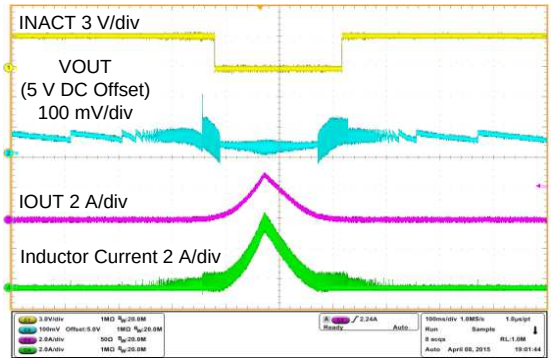
VIN = 2.8 V to 3.3 V, VOUT = 5 V, IOUT = 2 A, Cff = 10 pF

Figure 26. Line Transient Response with Cff



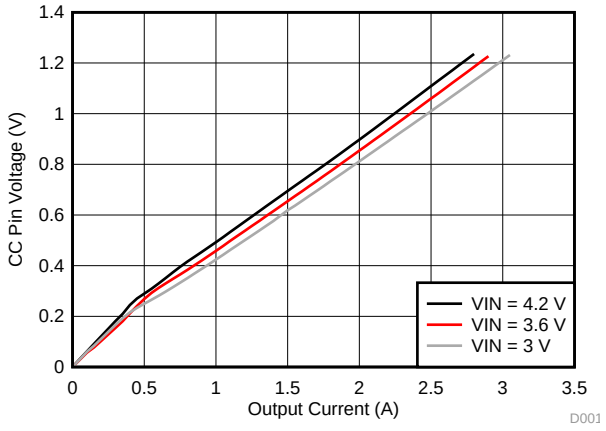
VIN = 3.6 V, VOUT = 5.1 V, R_{CC} = 41.2 kΩ, R_L = 2.5 Ω to 1.5 Ω

Figure 27. Constant Current Response



VIN = 3.6 V, VOUT = 5 V, CC = 3.0 A, IOUT from 0 mA to 3 A

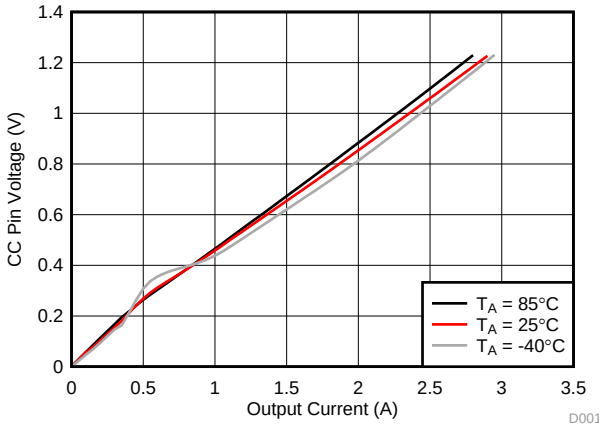
Figure 28. Load Sweep



R_{CC} = 41.2 kΩ (CC current set to 3 A), T_A = 25°C

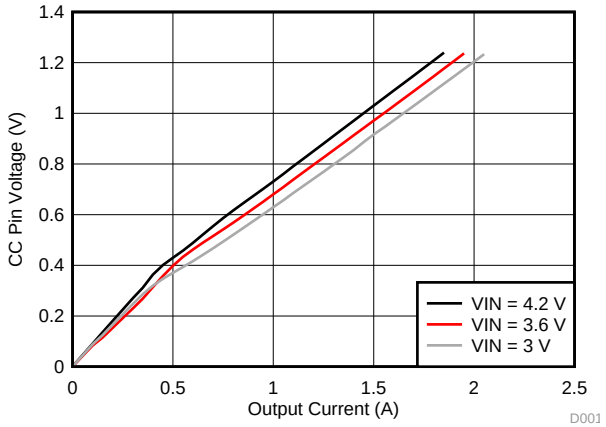
Figure 29. CC Pin Voltage vs Output Current with Different Inputs

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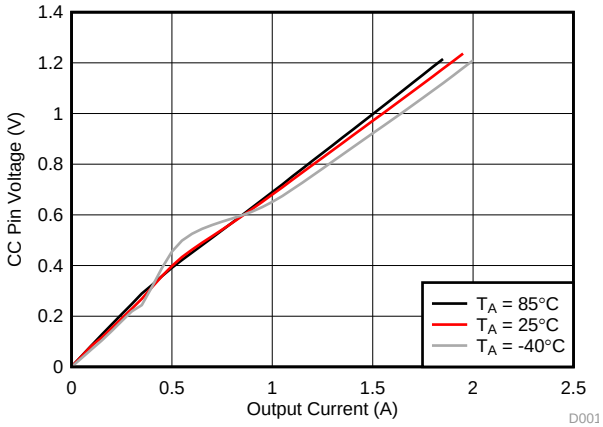
R_{CC} = 41.2 kΩ (CC current set to 3 A), V_{IN} = 3.6 V

Figure 30. CC Pin Voltage vs Output Current with Different Ambient Temperatures



R_{CC} = 61.9 kΩ (CC current set to 2 A), T_A = 25°C

Figure 31. CC Pin Voltage vs Output Current with Different Inputs



R_{CC} = 61.9 kΩ (CC current set to 2 A), V_{IN} = 3.6 V

Figure 32. CC Pin Voltage vs Output Current with Different Ambient Temperatures

9.2.2 TPS61236P 2.3-V to 5-V Input, 5-V 2-A Output Converter

In this application, the TPS6123x is required to be used as a standard boost converter to output 5-V voltage and maximum 2-A current. The Constant Current function should be disabled, and the INACT function is not needed either.

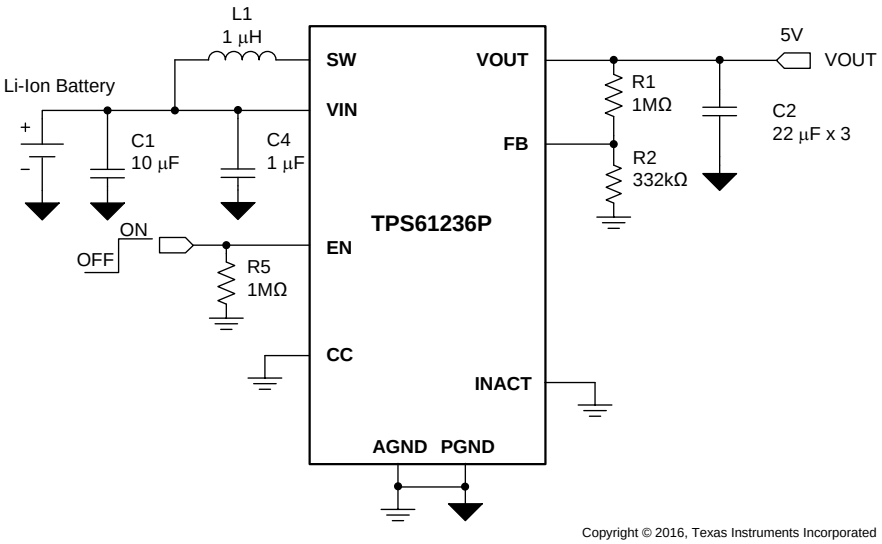


Figure 33. TPS61236P 5-V 2-A Output Typical Application

9.2.2.1 Design Requirements

The design parameters for the TPS61236P 5-V output current design are listed in Table 4.

Table 4. TPS61236P 5-V Output Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	2.3 V to 4.4 V
Output voltage	5 V
Output current rating	2 A
Operating frequency	1 MHz

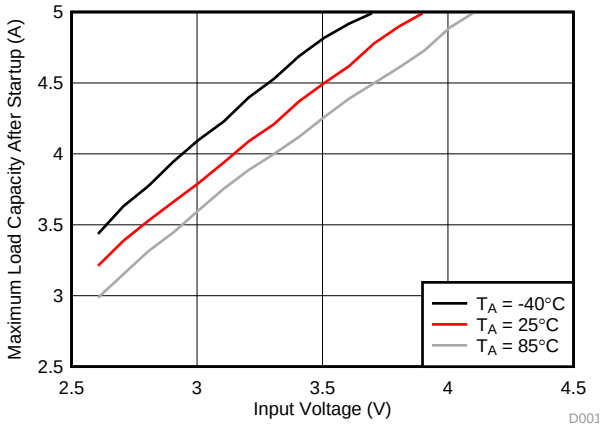
9.2.2.2 Detailed Design Procedure

Refer to the *Detailed Design Procedure* section for the detailed design steps.

Because the CC function and the INACT function are not needed, the user can simply connect the two pins to ground to disable the functions as shown in Figure 33.

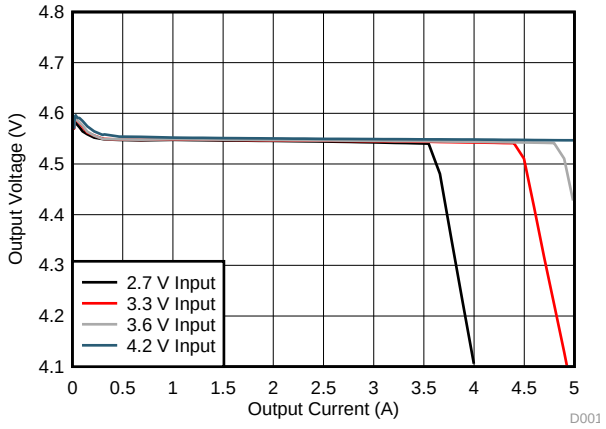
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9.2.2.3 TPS61236P 5-V Output Application Curves



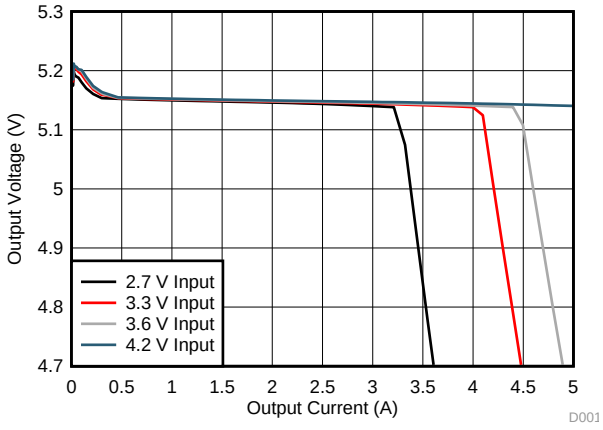
V_{OUT} = 5.1 V (TPS61235P), CC pin connected to GND

Figure 34. Maximum Load Capability after Startup



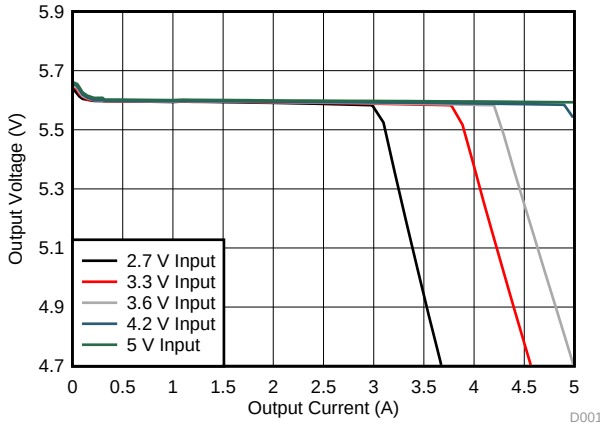
V_{OUT} = 4.5 V (TPS61236P), CC pin connected to GND

Figure 35. Load Regulation



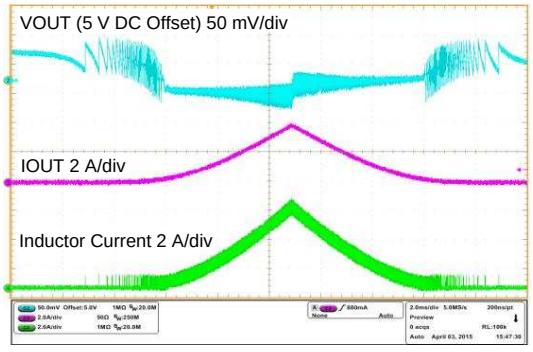
V_{OUT} = 5.1 V (TPS61235P), CC pin connected to GND

Figure 36. Load Regulation



V_{OUT} = 5.5 V (TPS61236P), CC pin connected to GND

Figure 37. Load Regulation



V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} from 0 mA to 4 A

Figure 38. Load Sweep

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.3-V and (V_{OUT} – 0.6)-V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47-µF is a typical choice in this circumstance.

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11 Layout

11.1 Layout Guidelines

For all switching power supplies, layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control/analog ground to minimize the effects of ground noise. Connect these ground nodes near the ground pins of the IC. The most critical current path for all boost converters is from the switching FET, through the synchronous FET, the output capacitors, and back to the ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the VOUT and PGND pins of the IC.

See Figure 39 for the recommended layout.

11.2 Layout Example

The bottom layer is a large GND plane connected by vias.

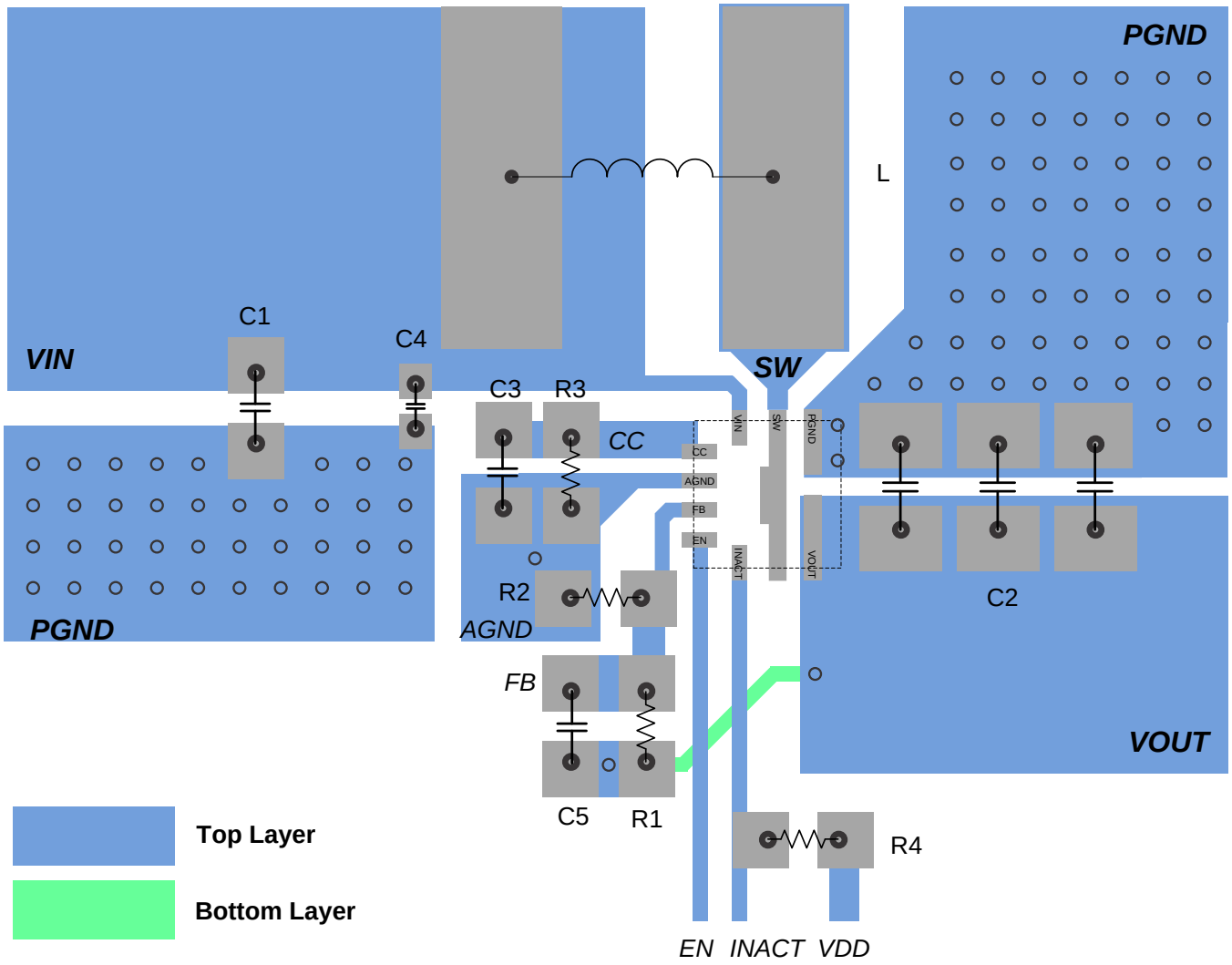


Figure 39. Layout Recommendation

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum power dissipation limit is determined using:

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \quad (9)$$

Where:

T_A is the maximum ambient temperature for the application.

$R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table.

The TPS6123x handles high power conversion so requires special attention to the power dissipation. The junction-to-ambient thermal resistance of a package in an application greatly depends on the PCB type and layout, and many system-dependent factors such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components also affect the power-dissipation limits.

Two common basic approaches to enhancing thermal performance are listed below.

- Increase the power dissipation capability of the PCB. It is necessary to have sufficient copper area as heat sinks. For DC voltage nodes like VIN, VOUT, and PGND, make the copper area as large as possible. Multiple vias are helpful in further reducing thermal stress. It is also a good practice to have thick copper layers in order to minimize the PCB conduction loss and thermal impedance.
- Introduce airflow in the system.

For more details on how to use the thermal parameters in the Thermal Information table, check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

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12 Device and Documentation Support

12.1 Device Support

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12.2 Documentation Support

12.2.1 Related Documentation

Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor Application Report (SLVA289)

Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report (SZZA017)

Semiconductor and IC Package Thermal Metrics Application Report (SPRA953)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61235P	Click here	Click here	Click here	Click here	Click here
TPS61236P	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61235PRWLR	ACTIVE	VQFN-HR	RWL	9	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZGEI	Samples
TPS61235PRWLT	ACTIVE	VQFN-HR	RWL	9	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZGEI	Samples
TPS61235RWLR	ACTIVE	VQFN-HR	RWL	9	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZBBI	Samples
TPS61235RWLT	ACTIVE	VQFN-HR	RWL	9	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZBBI	Samples
TPS61236PRWLR	ACTIVE	VQFN-HR	RWL	9	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZGFI	Samples
TPS61236PRWLT	ACTIVE	VQFN-HR	RWL	9	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZGFI	Samples
TPS61236RWLR	ACTIVE	VQFN-HR	RWL	9	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZBCI	Samples
TPS61236RWLT	ACTIVE	VQFN-HR	RWL	9	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZBCI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

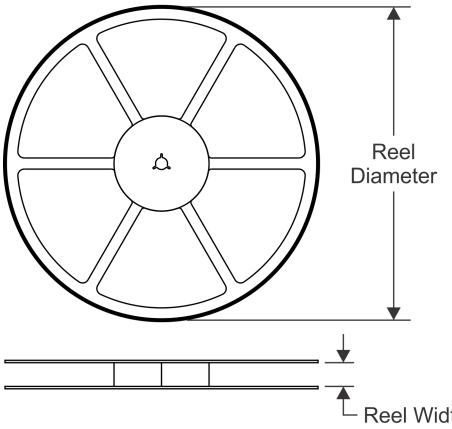
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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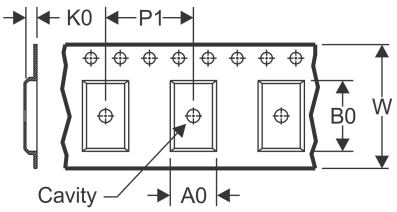
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

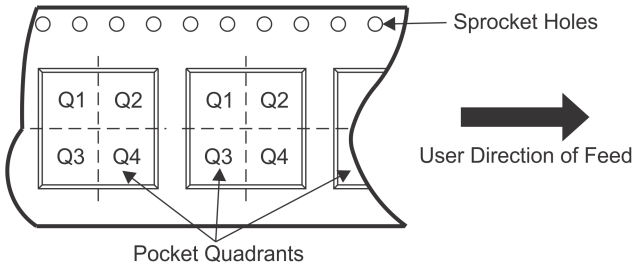


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

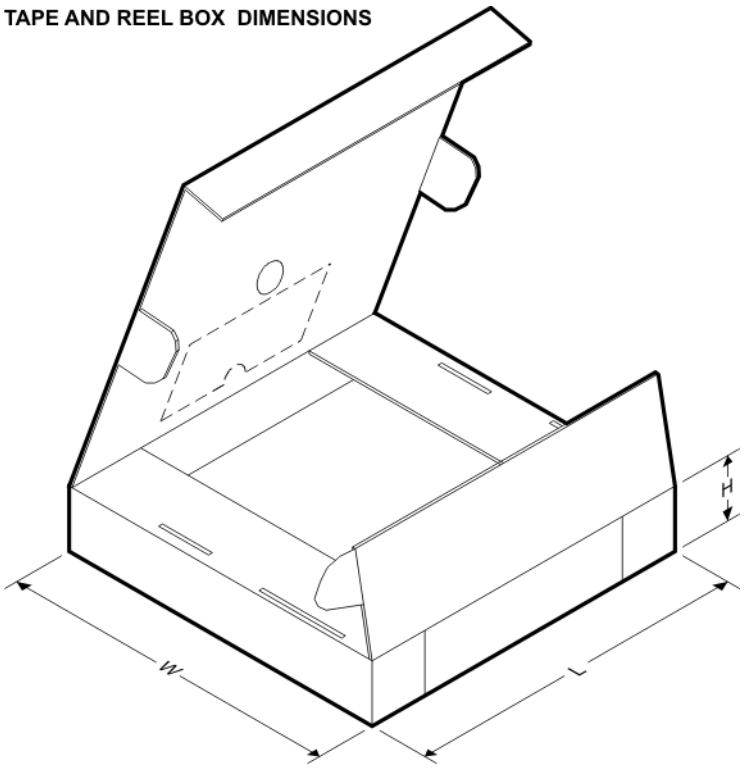
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61235PRWLR	VQFN-HR	RWL	9	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS61235PRWLT	VQFN-HR	RWL	9	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

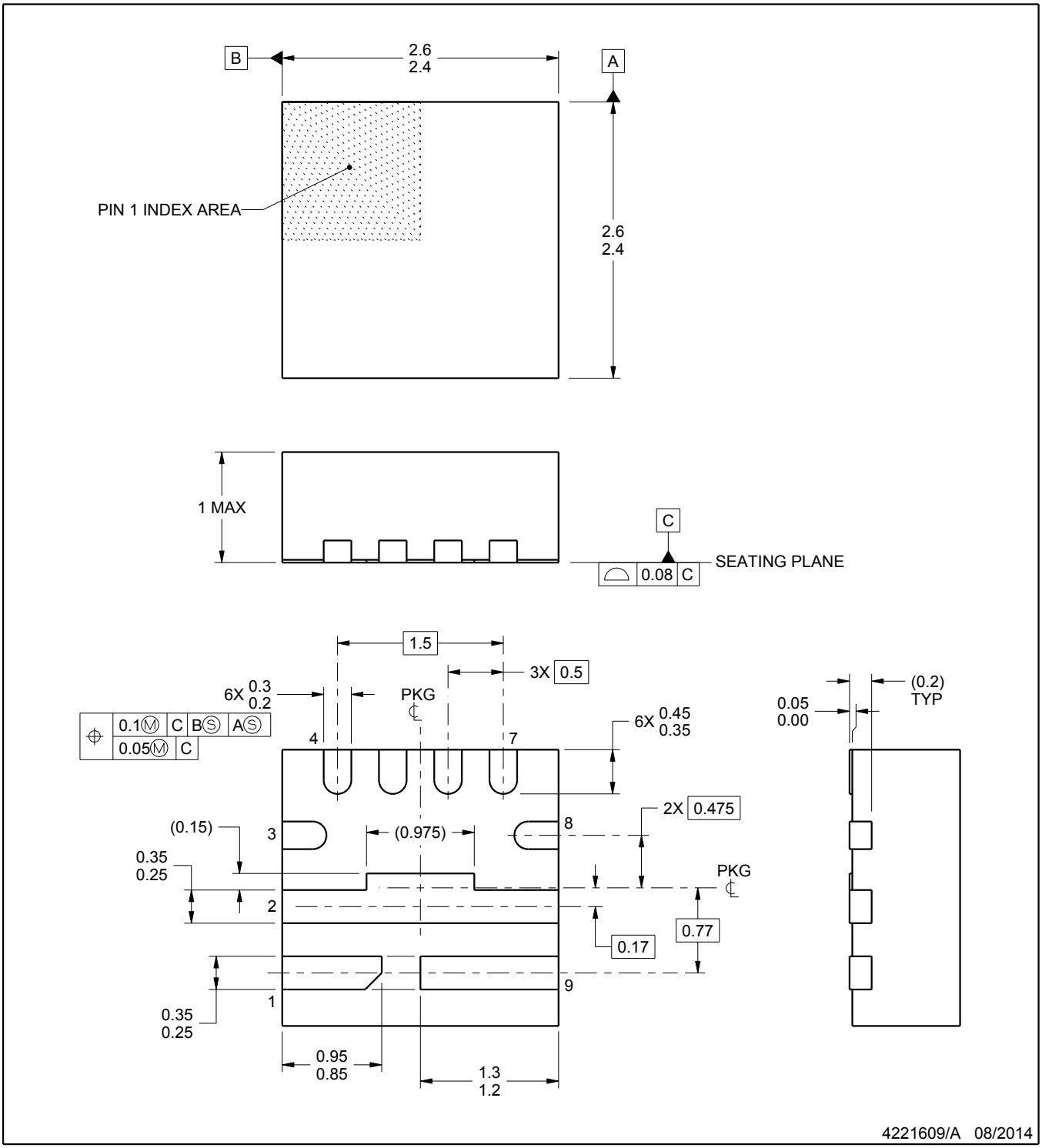
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61235PRWLR	VQFN-HR	RWL	9	3000	210.0	185.0	35.0
TPS61235PRWLT	VQFN-HR	RWL	9	250	210.0	185.0	35.0

PACKAGE OUTLINE

RWL0009A

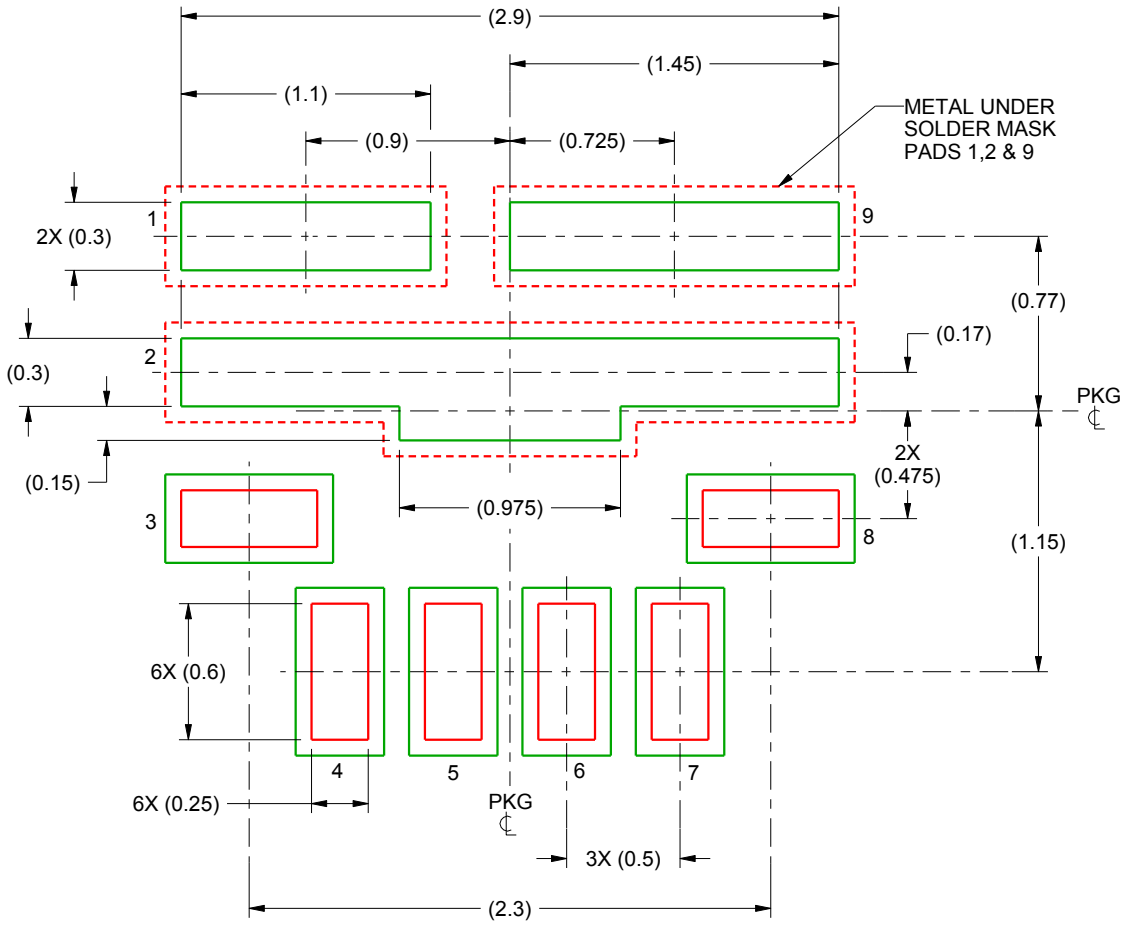
VQFN - 1 mm max height

QUAD FLAT PACK - NO LEAD

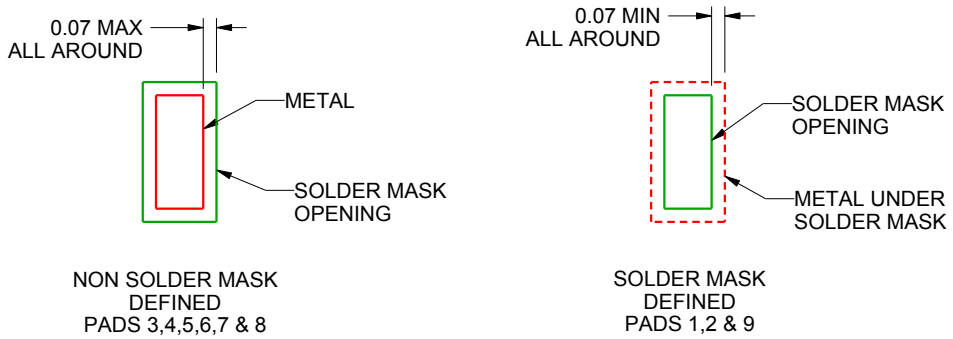


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

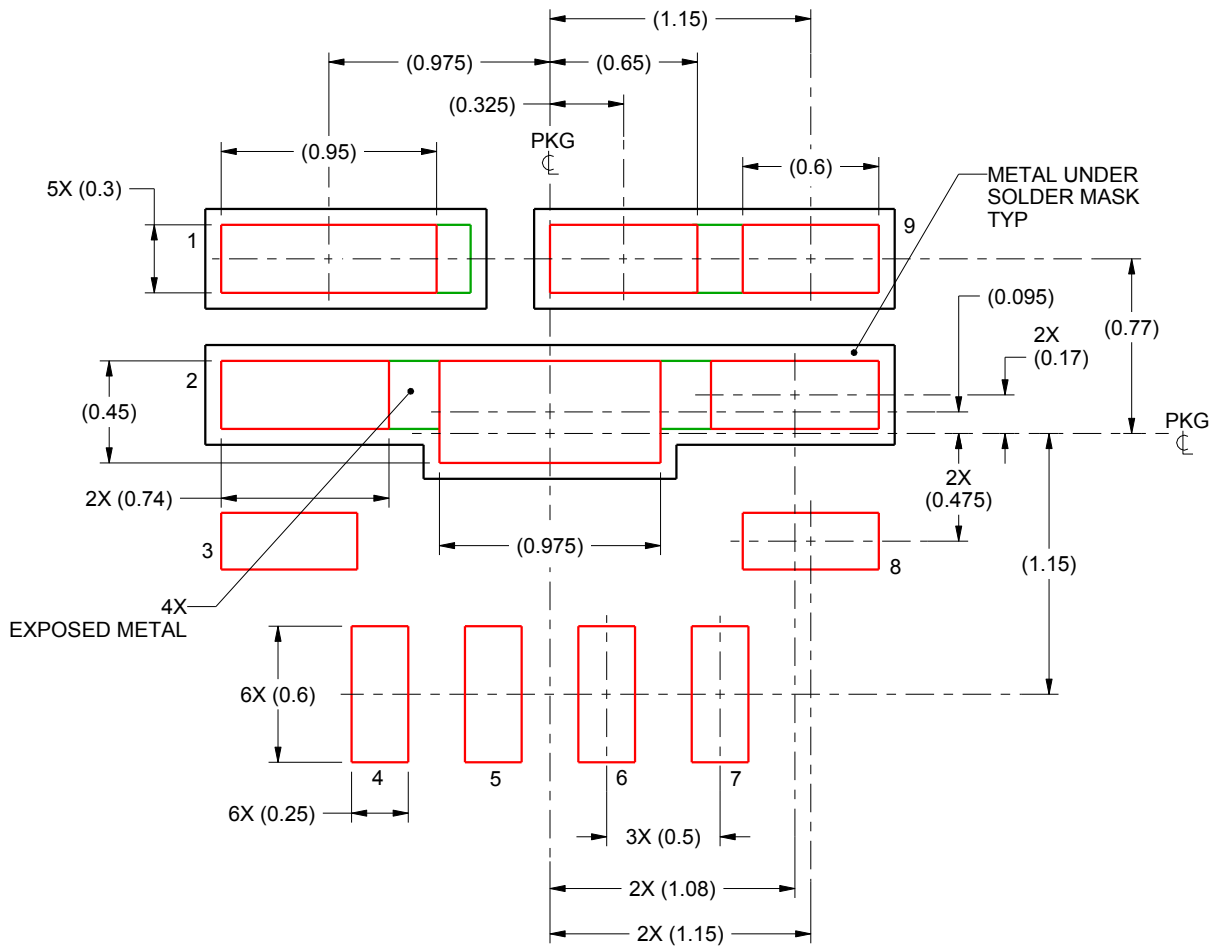


SOLDER MASK DETAILS

4221609/A 08/2014

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PADS 1,2 & 9
86% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

4221609/A 08/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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